LESSON PLAN

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
1	28/6/2016	Introduction to logic families	1	Black Board		
2	29/6/2016	CMOS logic		"		
3	30/6/2016	CMOS steady state electrical behaviour		"		
4	1/7/2016	CMOS dynamic electrical behaviour		"		
5	5/7/2016	CMOS logic families.		"		
6	7/7/2016	bipolar logic		"		
7	8/7/2016	diode logic Transistor logic		"		
8	12/7/2016	TTL families		"		
9	13/7/2016	TTL families		"		
10	14/7/2016	CMOS/TTL interfacing		"		
11	15/7/2016	CMOS logic and interfacing		"		
12	19/7/2016	emitter coupled logic		"		
13	20/7/2016	Comparison of logic families		"		
14	21/7/2016	Design and analysis procedure of decoder	2	"		
15	22/7/2016	decoder		"		
16	26/7/2016	encoder		"		
17	27/7/2016	design and analysis of encoder		"		
18	28/7/2016	Three state devices		"		
19	29/7/16	Multiplexers		"		
20	2/8/16	Multiplexer		"		

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Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
21	3/8/16	demultiplexers		Black Board		
22	4/8/16	Ex-OR gates and parity circuit		"		
23	5/8/16	Comparators		"		
24	9/8/16	Design of Comparator IC		"		
25	10/8/16	VHDL Modeling of decoders		"		
26	11/8/16	VHDL Modeling of decoders		"		
27	12/8/16	VHDL of encoders		"		
28	16/8/16	VHDL of multiplexers		Black Board		
29	17/8/16	VHDL of Multiplexers		"		
30	18/8/16	VHDL of Comparators		"		
31	19/8/16	Design Procedure of adders	UNIT -3	"		
32	23/8/16	Design and Analysis procedure of adders		"		
33	24/8/16	Design and Analysis of subtractor		"		
34	26/8/16	Design and Analysis of subtractor		"		
35	30/8/16	Analysis of ALU's		"		
36	31/8/16	Analysis of ALU		"		
37	1/9/16	barrel shifters		"		
38	2/9/16	simple floating point encoders		"		
39	6/9/16	simple floating point encoders		"		
40	7/9/16	dual parity encoders		"		

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Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
41	8/9/16	Cascading Comparator & Mux		Black Board		
42	9/9/16	cascading comparator & Mux		"		
43	13/9/16	VHDL Modeling of adders		"		
44	14/9/16	VHDL Modeling of adders		"		
45	15/9/16	VHDL modeling of subtractors		"		
46	16/9/16	VHDL Modeling of subtractors		"		
47	20/9/16	VHDL Modeling of barrel shifter		"		
48	21/9/16	VHDL modeling of barrel shift		"		
49	22/9/16	VHDL Modeling of Combinational Mux		"		
50	23/9/16	VHDL Modeling of Combinational Mux		"		
51	27/9/16	Latches	4	"		
52	28/9/16	Flip Flops		"		
53	29/9/16	Flip Flops		"		
54	30/9/16	Flip Flops		"		
55	4/10/16	Counters		"		
56	5/10/16	Counters		"		
57	6/10/16	Counters		"		
58	7/10/16	shift register		"		
59	13/10/16	shift register		"		
60	14/10/16	Synchoronous design Methodology		"		

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Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
61	18/10/16	Synchronous design Methodology		Black Board		
62	19/10/16	impediments to synchronous design		"		
63	20/10/16	Impediments to synchronous design		"		
64	21/10/16	VHDL Modeling of ripple counter		"		
65	25/10/16	VHDL Modeling of Synchronous counter		"		
66	26/10/16	VHDL of shift registers		"		
67	27/10/16	Introduction to PROM	5	"		
68	28/10/16	, RAM		"		
69	1/11/16	Introduction to PLA		"		
70	2/11/16	Design of PAL		"		
71	3/11/16	Introduction to CPLD		"		
72	4/11/16	Introduction to FPGA		"		
73	8/11/16	Design consideration of PLDS		"		
74	9/11/16	Design consideration of PLDS		"		
75	10/11/16	VHDL Modeling of Memories		"		
76	11/11/16	VHDL Modeling of PLD		"		